Dhanalakshmi Srinivasan Engineering College , Perambalur

Department of EEE

QUESTION BANK

Digital Logic Circuits

Unit -1
Boolean algebra and Combinational circuits

Part-A

1. State De-Morgan's law
2. What are the basic digital logic gates?
3. Define combinational logic
4. What are the features of gray code?
5. Which gates are called as the universal gates? What are its advantages?
6. Design Half adder
7. Design full adder
8. What is a Decoder?
9. Mention the uses of decoder.
10. What is an Encoder?
11. What is a priority encoder?
12. What is binary encoder?
13. Define multiplexer?
14. What is a demultiplexer?
15. What do you mean by comparator?
16. Name the two canonical forms for Boolean algebra.
17. What is the BCD equivalent for the gray code 1110?
18. For the given function, write the Boolean expression in product of maxterm form
    f(a,b,c)= m(2,3,5,6,7).
19. What is a data selector?
20. Write the logic equation and draw the internal logic diagram for a 4 to 1 mux.
21. Expand the function f (A, B, C) =A +B'C to standard SOP form?
22. Using k-map find minimum sop for the function.
    F (a, b, c) = m (0, 1, 5, 6, 7)
23. Implement the given function in 4:1 mux f= m(0,1,3,5,6)
24. Draw a combinational logic circuit, which can compare whether two bits binary numbers are same or not?
25. Convert $(1029)_{10}$ to Gray code.
26. Convert 53_{10} to excess – 3 code.
27. Define magnitude comparator?
28. Convert gray code 101011 into its binary equivalent.
29. Convert 10111011 is binary into its equivalent gray code.
30. Convert $(367)_{10}$ into Excess- 3 Code.

Part-B

1. State and prove De - Morgan's theorems using two variables.
2. Design a 4 bit Binary to gray code converter.
3. Realize the functions of NOT, AND ,OR and NAND gates only with NOR gates.
4. Convert the decimal 65 to BCD, Excess-3 and Gray code.
5. Encode data bits 1001 into a seven bit even parity Hamming code.
6. Design a two – bit magnitude Comparator.
7. Simplify the following Boolean function in SOP and POS form using K-map
   F (A,B,C,D) = **Σm(3,4,9,13,14,15) + Σd (2,5,10,12)**
8. Simplify the following function using K-Map and Quine McCluskey methods.
   F =m0+m2+m4+m8+m9+m10+m11+m12+m13 Implement the result using NAND gates.
9. Design a Half subtractor using NAND- NAND logic
10. Design a four bit gray to binary code converter.

11. Design 1 to 4 demux.
12. Draw and explain the working of a carry look ahead adder.
13. Explain the different types of Parity checking methods.
14. Explain the operation of 2 bit magnitude comparator.
15. Implement a full adder circuit using (i) Decoder (ii) Multiplexer
16. Construct a combinational circuit to convert BCD to EX-3 code.
17. Design a Full Adder and a Full Subtractor.
18. Draw and explain the working of 4 bit adder – subtractor circuit.
19. Simplify F (A,B,C,D) = **Σm (1,3,5,8,9,11,15) + Σd (2,13).**If don't care conditions are not taken into care what will be the simplified Boolean function? Write your comments on it. Implement both circuits using logic gates.
20. Simplify the following function using Quine McCluskey method.
    F (A,B,C,D) = **Σm(0,1,3,4,6,8,11)**

Unit 2

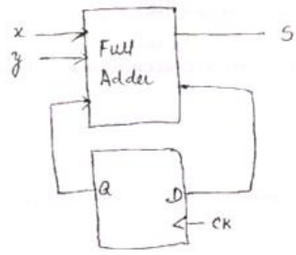
Synchronous Sequential circuits

Part A

1. Define sequential circuit?
2. Write the characteristic equations for JK and D Flip Flops.
3. If the input frequency of T FF is 1600 kHz, what will be the output frequency?
4. How can a D flip flop be converted into T flip-flop?
5. What is meant by the term edge triggered?
6. Give the state diagram of JK ff?
7. Draw the logic diagram of Master Slave JK ff?
8. Write the characteristic equation of JK ff and show JK ff can be converted into T ff
9. How many ff's are required to design a mod-7 up down counter?
10. Difference between Moore & mealy type sequential circuits
11. Distinguish between combinational & sequential logic circuits
12. What are the classification of sequential circuits?
13. What is Flip flop? Mention the different types of Flip Flops.
14. What is a master-slave flip-flop?
15. Define registers.
16. Define shift registers.
17. Define state table.

Part B

1. A sequential circuit has 2D ff's A and B an input x and output y is specified by the following next state and output equations.
   A (t+1)= Ax + Bx
   B (t+1)= A'x
   Y= (A+B) x'
   (i) Draw the logic diagram of the circuit.
   (ii) Derive the state table.
   (iii) Derive the state diagram.
2. Design a mod-6 counter FF'S. Draw the state transition diagram of the same.
3. Draw the clocked RS FF and explain with truth table.
4. Write the excitation tables of SR, JK , D, and T Flip flops.
5. (i)Summarize the design procedure for synchronous sequential circuit.
   (ii)Realize D and T flip flops using JK flip flops.
6. Design a synchronous decade counter using D Flip Flop.
7. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full adder circuit connected to a D flip-flop, as shown below. Derive the state table and state diagram of the sequential circuit.



8. Reduce the number of states in the following state table and tabulate the reduced state table.

Present state	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

   Starting from state a, and the input sequence 01110010011, determine the output sequence for the given and reduced state stable.
9. Design and explain the working of mod-10 up –down counter using JK ff. write excitation table and state table.
10. Explain the working of master slave JK FF. What are its advantages.
11. Explain the shift Register.

Unit 3
Asynchronous Sequential circuits

Part A

1. What are the assumptions made for pulse mode circuit.
2. Distinguish between synchronous and asynchronous sequential circuits
3. What is an essential hazard and how to eliminate it?
4. What is race around condition?
5. What are the different modes of operation in asynchronous sequential circuits?
6. Define static 0 and static 1 hazard?
7. Distinguish between pulse mode and fundamental mode asynchronous sequential circuits.
8. What is meant by state assignment?
9. What are races?
10. What is non critical race?
11. What is critical race?
12. What is a cycle?
13. Explain Dynamic hazard.
14. What are the different techniques used in state assignment?
15. Write short note on shared row state assignment.
16. Write short note on one hot state assignment.

Part B

1. Design an asynchronous sequential circuit that has 2 inputs x2 and x1, and one output z. the output is to remain a 0 as long as a 0.the first change in x2 that occurs while x1 is a1 will cause z to be a1. z is to remain a1 until x1 returns to 0. Construct a state diagram and flow table. Determine the output equations.
2. Draw the fundamental mode and pulse mode asynchronous sequential circuits and explain in detail.
3. Obtain the primitive flow table for an asynchronous circuit that has 2 input's x, y and output z. an output z=1, is to occur only during the input state xy=01 and then if and only if the input state xy=01 is preceded by the input sequence xy=01, 00, 10,00,10,00
4. Design a circuit with input a and b to give an output z=1 when AB =11 but only if A becomes 1 before B, by drawing total state diagram, primitive flow table and output map in which transient state is included.
5. Explain with neat diagram the different hazards and the way to eliminate them.
6. Explain in detail about Races.
7. Explain the different methods of state assignment

8. Design an asynchronous decade counter using JK Flip Flop.
9. Minimize the following state table.

	NS,X	
	X	
P.S	0	1
A	A, 0	D, 0
B	C, 1	D, 0
C	B, 0	A, 1
D	D,1	A,1
E	D,1	A,1
F	D,0	A,0
G	D,1	A,1
H	D,1	C,1

Unit 4

Programmable logic devices, Memory and logic families

Part A

1. Mention the two types of erasable PROM?
2. What is PLA?
3. What are the difference between PLA and PAL?
4. What is the major difference between ECL and TTL?
5. What is meant by static and dynamic memories?
6. Define the terms fan out, fan in?
7. What is the advantage of schottky TTL family?
8. List out the advantage and disadvantage of dynamic RAM cell?
9. Give the classification of logic families
10. What is propagation delay?
11. Define noise margin?
12. What are the types of TTL logic?
13. What is depletion mode operation MOS?
14. What is an enhancement mode operation of MOS?
15. Explain ROM and mention the different types of ROM.
16. Define PLD. Give the classification of PLD.
17. What is FPGA?

Part B

1. Draw a dynamic ram cell and explain its operation. Compare its simplicity that of NMOS static RAM cell, by way of diagram and operation.
2. Discuss on the concept of working and applications of following memories.
   i) ROM
   ii) EPROM
   iii) PLA.
3. Explain the basic structure of 256 x 4 static RAM with neat sketch.
4. A combinational circuit is defined by the functions.
   F1 (a, b, c) = _ (3, 5, 6, 7)
   F2 (a, b, c) = _ (0, 2, 4, 7) implement the circuit with a PLA.
   ii). Implement the given function using PAL and PLA.
   F1 = _ (0, 1, 2, 4, 6, 7)
   F2 = _ (1, 3, 5, 7)
   F3= _ (0, 2, 3, 6)
5. Write short notes on semiconductor memories.
6. Explain with neat diagrams TTL, ECL,and CMOS digital logic families.
7. Discuss all the characteristics of digital IC's.
8. Write notes on FPGA.

Unit 5
VHDL

Part A

1. State the features of register transfer logic.
2. What is micro-operation.
3. What is macro-operation.
4. What is VHDL?
5. Give the features of VHDL.
6. What is package in VHDL?
7. What do you mean by signal in VHDL?
8. What do you mean by variable in VHDL?
9. Explain CASE statement with example.
10. Explain CASE statement with example.

Part B

1. Write VHDL code for a four-bit register.
2. Write VHDL code for (i) 3:8 decoder
   (ii) Decimal to BCD encoder
   (iii) Priority encoder
   (iv) 8:1 Multiplexer
3. Write VHDL code for (i) 2 bit comparator
   (ii) 4 bit adder
   (iii) 4 bit subtractor
4. Write VHDL code for a serial adder using Mealy-type FSM .
5. Write VHDL code for a serial adder using Moore-type FSM .
6. Write VHDL code that represents a modulo-10 up counter with synchronous reset.